

WHAT IS CLAIMED IS:

2 1. In a wire-bond package arrangement including a
3 substrate; at least one semiconductor chip mounted on
4 said substrate; and at least one each of a power ring, a
5 ground ring and a signal ring at the height of the
6 substrate surfaces mounting said at least one chip being
7 operatively connected to circuitry on said chip by wires;
8 the improvement comprising:

9 a) said at least one power ring and ground
10 ring being located in an interstitial
11 pattern on the surface of said substrate;

12 b) a first wire extending within a vertical
13 height between the surface of the
14 substrate and the surface of said chip
15 said wire commonly interconnecting said
16 interstitial pattern formed by said at
17 least one power and ground ring with
18 circuitry on said chip; and

19 c) a second wire extending in a vertical loop
20 spaced above said first vertical wire loop
21 and interconnecting circuitry on said chip
22 with said at least one signal ring.

1 -2. A wire-bond package arrangement as claimed in Claim
2 1, wherein said chip, and said first and second wires on
3 said substrate are encapsulated with an encapsulant so as
4 to form a low-profile wire-bond package arrangement of
5 specified overall height.

1 3. A wire-bond package arrangement as claimed in Claim
2 1, wherein said at least one power ring comprises a
3 voltage bus and said at least one ground ring comprises a
4 ground bus, wherein the interstitial pattern of said
5 buses enables the provision of a single row of wire-bond
6 connections on the substrate to simulate a single ring.

1 4. A wire-bond package arrangement as claimed in Claim
2 2, wherein said arrangement comprises a chip-up package
3 having a reduced height wire loop to facilitate forming
4 of an increased thickness of an encapsulant over said
5 chip wires while maintaining the overall height of said
6 package arrangement within specified parameters.

1 5. A wire-bond package arrangement as claimed in Claim
2 2, wherein said arrangement comprises a cavity-down
3 plastic ball grid array package having a reduced height
4 of wire loop to facilitate forming of an increased
5 thickness of encapsulant over said chip and wires while
6 maintaining the overall height of said package within
7 specified parameters.

1 6. A wire-bond package arrangement as claimed in Claim
2 3; wherein there is provided a second voltage bus; and a
3 second signal wire-bond ring with interstitial power
4 connections facilitating the connection thereof with
5 circuitry on said chip through a second wire loop formed
6 by a third wire extending in elevation spaced above said
7 second wire forming said first wire loop.

1 7. A wire-bond package arrangement as claimed in Claim
2 6, wherein said chip, said first wire and said first and
3 second wire loops formed by said second and third wire-
4 bond wires are encapsulated with an encapsulant so as to
5 form a low-profile wire-bond package of specified overall
6 height.

1 8. In a method of forming a wire-bond package
2 arrangement including a substrate; at least one
3 semiconductor chip mounted on said substrate; and at
4 least one each of a power ring, a ground ring and a
5 signal ring at the height of the substrate surfaces
6 mounting said at least one chip being operatively
7 connected to circuitry on said chip by wires; the
8 improvement comprising:

- 9 a) locating said at least one power ring and
10 ground ring being located in an
11 interstitial pattern on the surface of
12 said substrate;
13 b) having a first wire extending in a
14 vertical height between the surface of the
15 substrate and the surface of said chip
16 said wire commonly interconnecting said
17 interstitial pattern formed by said at
18 least one power and ground ring with
19 circuitry on said chip; and
20 c) extending a second wire in a vertical loop
21 spaced above said first vertical wire loop
22 and interconnecting circuitry on said chip
23 with said at least one signal ring.

1 9. A method of forming a wire-bond package arrangement
2 as claimed in Claim 8, wherein said chip, and said first
3 and second wires on said substrate are encapsulated with
4 an encapsulant so as to form a low-profile wire-bond
5 package arrangement of specified overall height.

1 10. A method of forming a wire-bond package arrangement
2 as claimed in Claim 8, wherein said at least one power
3 ring comprises a voltage bus and said at least one ground
4 ring comprises a ground bus, wherein the interstitial
5 pattern of said buses enables the provision of a single
6 row of wire-bond connections on the substrate to simulate
7 a single ring.

1 11. A method of forming a wire-bond package arrangement
2 as claimed in Claim 9, wherein said arrangement comprises
3 a chip-up package having a reduced height wire loop to
4 facilitate forming of an increased thickness of an
5 encapsulant over said chip wires while maintaining the
6 overall height of said package arrangement within
7 specified parameters.

1 -12. A method of forming wire-bond package arrangement as
2 claimed in Claim 9, wherein said arrangement comprises a
3 cavity-down plastic ball grid array package having a
4 reduced height of wire loop to facilitate forming of an
5 increased thickness of encapsulant over said chip and
6 wires while maintaining the overall height of said
7 package within specified parameters.

1 13. A method of forming a wire-bond package arrangement
2 as claimed in Claim 10, wherein there is provided a
3 second voltage bus; and a second signal wire-bond ring
4 with interstitial power connections facilitating the
5 connection thereof with circuitry on said chip through a
6 second wire loop formed by a third wire extending in
7 elevation spaced above said second wire forming said
8 first wire loop.

1 14. A method of forming a wire-bond package arrangement
2 as claimed in Claim 6, wherein said chip, said first wire
3 and said first and second wire loops formed by said
4 second and third wire-bond wires are encapsulated with an
5 encapsulant so as to form a low-profile wire-bond package
6 of specified overall height.